I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to : Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on

Karen Cody-Marcus 10/14/03

(Signature & date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :	October 14, 2003
Pogge et al. :	Group Art Unit:
Serial No. 10/605,204 :	Examiner:
Filed: 09-15-03 :	International Business Machines Corporation 2070 Route 52 Hopewell Junction, NY 12533

TITLE: INTEGRATED ELECTRONIC CHIP AND INTERCONNECT DEVICE AND PROCESS FOR MAKING THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, are attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,

Jay H. Anderson
Registration No. 38,371
Telephone No. 845-894-3667

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
FIS920020007	10/605,204
Applicant(s)	
Pogge et al.	
Filing Date	**Group Art Unit**
09-15-03	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		"Novel microelectronic packaging method for reduced thermomechanical stresses on low dielectric constant materials", Emery et al., Intel Corp.
		"Bridging the chip/package process divide", Pogge et al., IBM Microelectronics

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.